REMARKS:

Claim 8 is canceled without prejudice. Claims 1, 5 and 9-12 are amended, and new claims 21-32 are added. Claims 1-7, 9-12 and 21-32 are pending in the application. Reexamination and reconsideration of the application, as amended, are respectfully requested.

The title of the invention is objected to. In response, the applicant amends the title to read: "Semiconductor Device Having a Controlled Gate Shape and Method for Manufacturing the Same".

Claims 1, 5, 6, 8, 9, 11 and 12 were rejected as being anticipated by U.S. Pat. Pub. 2001/0045608 to Tseng et al. This rejection is respectfully traversed.

Claim 1 requires a semiconductor device having: a semiconductor substrate; a gate electrode formed on the semiconductor substrate through a gate dielectric layer; first and second impurity diffusion layers formed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them; a third impurity diffusion layer formed in a portion immediately below the gate electrode in the semiconductor substrate; and a sidewall dielectric layer formed on a side surface section of the gate electrode. The semiconductor structure described in Tseng is fundamentally different in that it is a stacked structure and do not have the "first and second impurity diffusion layers formed in the semiconductor substrate". The source and drain regions 16 are deposited polysilicon layers. Therefore, Tseng does not anticipate the present claims nor render then obvious.

Claims 1-3, 5-7, 9, 11 and 12 were rejected as being anticipated by U.S. Pat. No. 6,130,454 to Gardner et al. Claims 4 and 10 were rejected as being obvious over the '454 patent and U.S. Pat. No. 6,201,278 to Gardner et al. The applicant amends claim 1 to incorporate the subject matter of claim 8, which is canceled. Since claim 8 was not rejected based on the above two references, the applicant believes that claims 1-7 and 9-12 are now allowable.

The applicant also add new claim 21 which contains the subject matter of the original claims 1 and 11, and dependent claims 22-31 which correspond to the original claims 2-10 and 12. For reasons that follow, the applicant submits that these new claims are allowable.

The original claim 11 requires "wherein surfaces of the first and second impurity diffusion layers are formed at a position higher than a surface of the element isolation region." This is not shown in the '454 and '278 references. In the '454 reference, the surfaces of the first and second impurity diffusion regions 52 are lower than the surface of the element isolation regions 12. The '278 reference does not show the element isolation regions. Accordingly, new claims 21-31 are patentable over the cited references.

New claim 32 is supported by the drawings (e.g. Fig. 8) and the specification (e.g. page 15). This claim requires that "a width of the upper surface of the gate electrode substantially equals to a width of the groove." This feature is not described or suggested in any of the cited references. For example, in the Tseng reference, the wall 20 has a non-zero thickness at the top, resulting in the width of the upper surface of the electrode 24 being smaller than the width of the groove (see Figs. 5-9 therein). The Gardner '454 reference is similar in this respect (see Figs. 8 and 9a therein). The applicant believes that new claim 32 is allowable over the cited art.

The art made of record but not relied upon by the Examiner has been considered. However, it is submitted that this art neither describes nor suggests the presently claimed invention.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: September 5, 2002

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Version with markings to show changes made:

In the claims:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a gate electrode formed on the semiconductor substrate through a gate dielectric layer;

first and second impurity diffusion layers formed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them;

a third impurity diffusion layer formed in a portion immediately below the gate electrode in the semiconductor substrate; and

a sidewall dielectric layer formed on a side surface section of the gate electrode,

wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof, and

wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer.

5. (Amended) A semiconductor device according to [any one of] claim 1, wherein an element isolation region is formed in the semiconductor substrate.

9. (Amended) A semiconductor device according to [any one of] claim 1, wherein a metal silicide layer is formed on the first and second impurity diffusion layers, and the gate electrode includes a metal silicide layer on an upper surface thereof.

10. (Amended) A semiconductor device according to [any one of] claim 1, wherein the sidewall dielectric layer is formed from a material including, as a main component, silicon nitride, silicon oxide or a compound film thereof.

11. (Amended) A semiconductor device according to [any one of] claim 1, wherein surfaces of the first and second impurity diffusion layers are formed at a position higher than a surface of the element isolation region.

12. (Amended) A semiconductor device according to [any one of] claim 1, wherein the sidewall dielectric layer has an outer surface that is generally vertical with respect to the surface of the semiconductor substrate, and a film thickness that gradually reduces from a bottom thereof toward an upper surface thereof.